**REMARKS**

The claims are claims 1 to 4 and 11 to 14.

Claims 1 and 11 have been amended to further distinguish over the rejection.

Claims 1 to 4 and 11 to 14 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Kaneko (U.S. Patent No. 5,561,672) and applicant admitted prior art. The OFFICE ACITON states that Kaneko teaches the recited first buffer, second buffer and copy/access controller. The OFFICE ACTION states that the applicant admitted prior art teaches controllers that detect the empty and full state of a buffer and create control signals for the loading and emptying of the buffer.

Claims 1 and 4 recite subject matter not made obvious by the combination of Kaneko and applicant admitted prior art. Claim 1 recites a copy/access controller "operable to prompt said second component to access said second buffer when said data is copied from said first buffer." Claim 11 similarly recites "prompting said second component to access said data in said second buffer when said copying step is completed." These limitations are not made obvious by the combination of Kaneko and applicant admitted prior art. First, Kaneko includes no teaching regarding the timing and control of data movement between first buffer 21 and second buffer 29. Thus Kaneko cannot make obvious prompting the second component to transfer data from the second buffer following the copy operation. The applicant admitted prior art teaches triggering a read operation upon receipt of a full signal or a nearly full signal. However, claims 1 and 11 recite a different operation. The copy between the first buffer and the second buffer may be controlled by a full/nearly full signal as in the applicant admitted prior art. However, the applicant admitted prior art fails to teach or make obvious the second data transfer from the

second buffer to the second component prompted by completion of the copy operation. Accordingly, claims 1 and 11 are allowable over the combination of Kaneko and applicant admitted prior art.

Claims 1 and 11 recite further subject matter not made obvious by the combination of Kaneko and applicant admitted prior art. Claim 1 recites "said first buffer receiving and storing data received from said first component at said first clock rate" and "said second buffer supplying data recalled therefrom to said second component at said second clock rate." Claim 11 recites "transferring data from said first component to a first buffer operable at said first clock rate" and "prompting said second component to access said data in said second buffer at said second clock rate." Kaneko fails to teach two differing clock rates. There is no teaching of clock rates in Kaneko, thus first buffer 21 and second buffer 29 cannot operate at the differing rates recited in claims 1 and 11. The applicant admitted prior art teaches writing at one clock rate and reading at another clock rate from a single FIFO buffer 2. Accordingly, the combination of Kaneko and applicant admitted prior art fails to make obvious the differing clock rates of the first and second buffers recited in claims 1 and 11.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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